What is claimed is:

[Claim 1] 1. A synchronous memory device with a single port memory unit, the synchronous memory device comprising:

the single port memory unit for storing data according to a predetermined clock;

a configurable write buffer electrically connected to the single port memory unit for storing data according to the predetermined clock and for transferring its stored data to the single port memory unit according to the predetermined clock;

a write blocking logic electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the predetermined clock, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal; and

an arbiter electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

[Claim 2] 2. The synchronous memory device of claim 1, wherein the write blocking logic comprises:

a first counter for counting the remaining data storage capability of the configurable write buffer;

a write comparator electrically connected to the first counter for comparing the remaining data storage capacity of the configurable write buffer counted by the first counter with a first predetermined count value and controlling the configurable write buffer to store data;

a read comparator electrically connected to the first counter for comparing the remaining data storage capacity of the configurable write buffer counted by the first counter with a second predetermined count value and controlling the configurable write buffer to transfer its stored data to the single port memory unit;

a write select counter electrically connected to the first counter for counting how many data the configurable write buffer has ever stored and generating a write select value;

a read select counter electrically connected to the first counter for counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value;

and the configurable write buffer comprises:

a plurality of buffer modules for storing data;

a demultiplexer electrically connected to the buffer modules for storing data to one of the buffer modules according to the write select value; and

a multiplexer electrically connected to the buffer modules for transferring data stored in one of the buffer modules to the single port memory unit according to the read select value.

[Claim 3] 3. The synchronous memory device of claim 2, wherein the first counter has an initial count value equal to how many data the configurable write buffer can store and downward counts the remaining data storage capacity of the configurable write buffer, and the first predetermined count value is equal to zero.

[Claim 4] 4. The synchronous memory device of claim 3, wherein the write comparator controls the configurable write buffer to stop storing data when

comparing that the remaining data storage capacity of the configurable write buffer is equal to zero.

[Claim 5] 5. The synchronous memory device of claim 3, wherein the read comparator controls the configurable write buffer to stop transferring its stored data to the single port memory unit when comparing that the remaining data storage capacity of the configurable write buffer is equal to how many data the configurable write buffer can store.

[Claim 6] 6. The synchronous memory device of claim 2, wherein the write select counter downward counts how many data the configurable write buffer has ever stored and generates the write select value.

[Claim 7] 7. The synchronous memory device of claim 2, wherein the read select counter downward counts how many data the configurable write buffer has ever transferred to the single port memory unit and generates the read select value.

[Claim 8] 8. A synchronous\asynchronous memory device with a single port memory unit, the synchronous\asynchronous memory device comprising:

the single port memory unit for storing data according to a read clock;

a configurable write buffer electrically connected to the single port memory unit for storing data according to a write clock and for transferring its stored data to the single port memory unit according to the read clock;

a write blocking logic electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data

according to the write clock, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal; and

an arbiter electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

[Claim 9] 9. The synchronous\asynchronous memory device of claim 8, wherein the write blocking logic comprises:

a write counter for counting the remaining data storage capability of the configurable write buffer;

a read counter for counting how many data in the configurable write buffer ready to be transferred to the single port memory unit;

a read\write synchronizer electrically connected between the write counter and the read counter for changing signals synchronizing with the read clock to signals synchronizing with the write clock;

a write\read synchronizer electrically connected between the write counter and the read counter for changing signals synchronizing with the write clock to signals synchronizing with the read clock;

a write comparator electrically connected to the write counter for comparing the remaining data storage capacity of the configurable write buffer counted by the write counter with a first predetermined count value and controlling the configurable write buffer to store data;

a read comparator electrically connected to the read counter for comparing how many data in the configurable write buffer ready to be transferred to the single port memory unit with a

second predetermined count value and controlling the configurable write buffer to transfer its stored data to the single port memory unit according to the read clock;

a write select counter electrically connected to the write counter for counting how many data the configurable write buffer has ever stored and generating a write select value;

a read select counter electrically connected to the read counter for counting how many data the configurable write buffer has ever transferred to the single port memory unit and generating a read select value;

and the configurable write buffer comprises:

a plurality of buffer modules for storing data;

a demultiplexer electrically connected to the buffer modules for storing data to one of the buffer modules according to the write select value; and

a multiplexer electrically connected to the buffer modules for transferring data stored in one of the buffer modules to the single port memory unit according to the read select value.

[Claim 10] 10. A computer system comprising:

a first computer operating on a first clock;

a second computer operating on a second clock different from the first clock; and

a memory device comprising:

a single port memory unit for storing data according to the first clock;

a configurable write buffer electrically connected to the single port memory unit for storing data transferred from the first computer according to the first clock and for transferring its stored data to the single port memory unit according to the second clock;

a write blocking logic electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data transferred from the first computer according to the first clock, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal; and

an arbiter electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.